IN THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the above-referenced application:

1. (Canceled)

2. (Previously amended) The integrated circuit of claim 30, further comprising:

a plurality of conductive plugs formed in the substrate, the plugs providing a substantially low resistance path for electrically connecting the conductive layer to the isolation buried layer.

3. (Previously amended) An integrated circuit, comprising:

a first circuit section formed in a substrate;

a second circuit section formed in the substrate, the second circuit section being spaced laterally from the first circuit section;

an isolation buried layer formed under at least a portion of the first circuit section; and

a conductive layer formed on a surface of the integrated circuit and operatively coupled to the isolation buried layer at a plurality of points spaced throughout the buried layer, the conductive layer reducing an effective lateral resistance of the isolation buried layer to thereby increase an electrical isolation between the first and second circuit sections;

wherein the conductive layer comprises a plurality of conductive traces, the conductive traces intersecting with and connecting to one another to form a net.

4. (Currently amended) The integrated circuit of claim ~~1~~ 30, wherein the net includes a plurality of holes therein, at least a portion of the first circuit section being formed in one or more holes in the net.

5. (Currently amended) The integrated circuit of claim ~~1~~ 30, wherein the net overlays at least a portion of the first circuit section.

6. (Previously amended) The integrated circuit of claim 30, wherein the isolation buried layer is connected to a ground or reference source.

7. (Previously amended) The integrated circuit of claim 30, wherein the conductive layer is formed at least in part of metal.

8. (Previously amended) The integrated circuit of claim 30, further comprising:

a second isolation buried layer formed under at least a portion of the second circuit section; and

a second conductive layer formed on a surface of the integrated circuit and operatively coupled to the second isolation buried layer, the second conductive layer reducing an effective lateral resistance of the second isolation buried layer.

9. (Original) The integrated circuit of claim 8, further comprising:

a plurality of conductive plugs formed in the substrate, the plugs providing a substantially low resistance path for electrically connecting the second conductive layer to the second isolation buried layer.

10. (Original) The integrated circuit of claim 8, wherein the second conductive layer comprises:

a plurality of conductive traces, the conductive traces intersecting with and connecting to one another to form a second net.

11. (Original) The integrated circuit of claim 10, wherein the second net includes a plurality of holes therein, wherein at least a portion of the second circuit section is formed in one or more holes in the second net.

12. (Original) The integrated circuit of claim 10, wherein the second net overlays at least a portion of the second circuit section.

13. (Original) The integrated circuit of claim 8, wherein the first and second conductive layers are electrically connected to separate ground or reference sources.

14. (Original) The integrated circuit of claim 8, wherein:

the second circuit section comprises at least one bipolar transistor device, the bipolar transistor device including a collector buried layer formed in the substrate above the second isolation buried layer.

15. (Previously amended) The integrated circuit of claim 30, wherein:

the integrated circuit is a mixed signal integrated circuit;

the first circuit section comprises a digital circuit section; and

the second circuit section comprises an analog circuit section.

16. (Previously amended) The integrated circuit of claim 30, wherein the isolation buried layer has a lower resistivity than the substrate.

17. (Previously amended) The integrated circuit of claim 30, wherein the isolation buried layer is formed in the substrate at depth in a range from about 2 micrometers (μm) to about 5 μm from an upper surface of the substrate.

18. (Canceled)

19. (Canceled)

20. (Canceled)

21. (Canceled)

22. (Canceled)

23. (Canceled)

24. (Canceled)

25. (Canceled)

26. (Canceled)

27. (Canceled)

28. (Canceled)

29. (Canceled)

30. (Previously added) An integrated circuit, comprising:

a first circuit section formed in a substrate;

a second circuit section formed in the substrate, the second circuit section being spaced laterally from the first circuit section;

an isolation buried layer formed under at least a portion of the first circuit section; and

a conductive layer formed on a surface of the integrated circuit and operatively coupled to the isolation buried layer, the conductive layer reducing an effective lateral resistance of the isolation buried layer;

wherein the conductive layer comprises a plurality of conductive traces, the conductive traces intersecting with and connecting to one another to form a net.

31. (Previously added) An integrated circuit, comprising:

a first circuit section formed in a substrate;

a second circuit section formed in the substrate, the second circuit section being spaced laterally from the first circuit section;

a first isolation buried layer formed under at least a portion of the first circuit section;

a first conductive layer formed on a surface of the integrated circuit and operatively coupled to the isolation buried layer, the conductive layer reducing an effective lateral resistance of the first isolation buried layer;

a second isolation buried layer formed under at least a portion of the second circuit section; and

a second conductive layer formed on a surface of the integrated circuit and operatively coupled to the second isolation buried layer, the second conductive layer reducing an effective lateral resistance of the second isolation buried layer;

wherein at least one of the first conductive layer and the second conductive layer comprises a plurality of conductive traces, the conductive traces intersecting with and connecting to one another to form a net.